A SILICON MONOLITHIC TECHNOLOGY FOR 1-2 GHZ ANALOG SIGNAL PROCESSING

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Abstract

A silicon bipolar monolithic technology has been developed and used for processing analog signals in the 0.5 to 2.0 GHz range. The measured performance of an IQ multiplier phase detector is described as one component of an integrated costas demodulator.

Introduction

A silicon bipolar integrated circuit process has been developed for the fabrication of analog functions that operate at frequencies of 1 GHz and above. This process, called OAT for Oxide Aligned Transistor technology, is capable of high density circuit functions (1000 to 5000 devices per die) providing both high frequency and high accuracy performance.[1] Techniques of oxide well pseudo self registration, an arsenic emitter doped from a polycrystalline source, and thin film cermet resistors contribute directly to this capability. Oxide wells provide reduced transistor side wall capacitance, exceptionally thick field oxide for minimum interconnect parasitic capacitance, and a relaxation of critical masking and alignment requirements associated with micron device spacing and large die area circuitry. The arsenic emitter is doped from a polycrystalline source which is retained and patterned to form an ohmic contact to the emitter. This technique is chosen to alleviate the conventional yield sensitive washed emitter technique which is prone to incipient base-emitter shorts. The cermet thin film process is incorporated to obtain highly accurate and temperature stable resistors which have minimum parasitic capacitance to substrate.

This resulting technology base gives transistors with f_T values in the 3.5 to 5.0 GHz range and resistors which match to better than 0.1% with a parasitic substrate capacitance as small as 0.02 pf/mil^2 (or 0.1 pf for a 200 ohm resistor). This process is presently being employed for high frequency analog circuitry in the 0.5 to 2.0 GHz frequency range, with a Costas demodulator used as an initial circuit test vehicle. The analog multiplier from this demodulator is described in this paper.

Monolithic Process

In industry standard practice, each diffusion step is masked by a separate and independent photoresist-etch step. Each mask must be aligned very precisely to maintain minimum geometry construction. The limitations on minimum device dimensions are consequently a function of best routine alignment capability and worst case mask distortions, such as run-out. OAT minimizes these problems by using a thick oxide well, as shown in Figure 1, to prealign subsequent diffusions. In the case shown, one mask prealigns three diffusions.

Take for instance, the isolation diffusion. The isolation mask must be aligned anywhere within the region shown in Figure 2, to achieve "perfect alignment", etc., for the remaining two diffusions.

Two well structures are used in OAT:

- Deep well, prealigns
  - isolation diffusion
  - deep collector N+ diffusion
  - base diffusion
- Shallow well, prealigns
  - base contacts
  - base enhancement diffusion
  - emitter

The oxide well structure therefore provides:

- Smaller device dimensions and lower junction capacitance due to limited lateral diffusion,
- Smaller device dimensions for a given mask and alignment capability (providing higher complexity LSI),
- Lower junction capacitance due to the oxide side walls,
- Smaller base-collector junction area since base contacts can be placed at the edge of the base, and
- Improved radiation resistance due to the reduced PN junction area.

The industry standard for the emitter-base structure of microwave devices is a washed emitter in which the emitter diffusion and the emitter contact occur in the same oxide cut, thus producing a minimum emitter-base junction area. The basic problem with this technique is that the etch dip which is needed to remove the SiO_2 formed during the emitter diffusion also etches in a lateral direction. This enhances the incipient emitter-base short which exists when the contact metal is evaporated and alloyed, since this approach relies only on lateral diffusion of the emitter for protection and passivation of the emitter-base junction. This, in turn, reduces yield and high temperature reliability. This critical step is eliminated in OAT by using an arsenic doped polycrystalline emitter doping source, as shown in Figure 3.

A heavily arsenic doped polycrystalline film is deposited and patterned. The arsenic is driven in to form the emitter region. The doped poly is then covered with metal and forms the ohmic contact between the active emitter region and the metal contact. Thus the metal system never makes contact with the silicon and is separated from it by the thickness of the poly. Emitter-base leakages and shorts are substantially reduced by this approach.

Figure 4 shows the final device cross-section and top view. This includes the cermet thin film which is used both as a resistor and as a barrier between the Ti-Al interconnect and the semiconductor device. Also shown is the two level metal interconnect system which is available to be used with OAT. Typical device dimensions and electrical characteristics are shown in Tables 1 and 2.

Test Pattern Description

The circuit functions for a costas demodulator have been designed and fabricated. A block diagram is shown in Figure 5. The IQ multiplier and phase detectors are

implemented with the same circuit function, as shown schematically in Figure 6. This balanced, differentially coupled circuit relies heavily upon the inherent matching of both active and passive components. Laser trimming individual resistors can reduce equivalent input offsets of a few millivolts down into the microvolt level. This permits direct coupling in many applications and increases the dynamic range for balanced circuits as shown in Figure 6.

The costas demodulator was designed to operate at 500 MHz. The circuit of Figure 6 was tested as a phase detector up thru 4 GHz, giving the correct transfer characteristics. Additional measurements made on the multiplier phase detector are shown in Table 3.

Overview

Progress in the area of high frequency analog integrated circuits has been slow in the industry relative to that in the digital area, chiefly because the critical parameters of analog circuits are more difficult to control and reproduce than those parameters critical to digital circuits. In addition, the potential market for such high frequency analog functions applicable to military communication, electronic warfare, and radar systems, etc., being considerably more limited than for digital IC's as well as of a more customized/specialized nature, has not attracted any significant fundamental research and development activity in the industry. Third, prior to the establishment of advanced isoplanar type of bipolar LSI device technologies (such as OAT) having RF quality transistors available in integrated form, the fundamental capability did not exist to implement high frequency analog circuits above 100 MHz.

At this time, the OAT technology has been proven sufficiently to realistically contemplate the device limitations associated with the large scale integration of sophisticated analog functions on single chips. Apart from the obvious savings in size, weight, and cost, these integrated RF subsystems are expected to offer substantial performance advantages which will simplify the design of microwave systems, and offer increased capability as compared with conventional discrete and thin film hybrid approaches. The cost savings are expected to be particularly dramatic when the analog integrated circuits are used in systems which perform signal processing in many similar parallel paths, such as surveillance receivers and multiple access receivers. The size and weight savings will also be particularly beneficial to satellite and spacecraft applications for which performance per pound is a key parameter.

References

[1]Initially developed by TRW for digital applications with work sponsored by Air Force funding under contract F33615-73-C-1110, "Gigabit Logic Design".

TABLE 1 OAT Device Physical Dimensions

Emitter width (also emitter contact width	3μ or 4μ
Base contact width	4μ
Metal overlap over contact	2μ each side
Metal to metal spacing	2μ
Minimum size transistor (to isolation centerlines)	44μ x 55μ

TABLE 2 OAT Device Electrical Characteristics

Transistor 1

$f_T \geq 3.5\text{-}5$ GHz
$C_{CO} \simeq 0.14$ pF at $V_{CB} = 0$ volts
$C_{EO} \simeq 0.08$ pF at $V_{EB} = 0$ volts
$C_{CS} \simeq 0.16$ pF at $V_{CS} = -3$ volts
$I_C \simeq 2$ mA
$r_c \simeq 60$ ohms

TABLE 3 Multiplier Measured Performance

Operating frequency	dc to > 2 GHz
Input level	≃ 40 mvpp
Differential mode gain	24.6 db
Common-mode gain	-32 db
Dynamic range	41 db
Power supply rejection	85 db
DC power	± 9 volts @ 7.3 ma

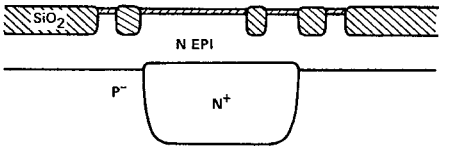

Figure 1 OAT Deep Well Structure

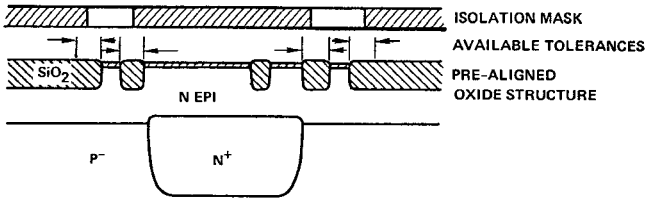

Figure 2 Alignment of the Isolation Mask

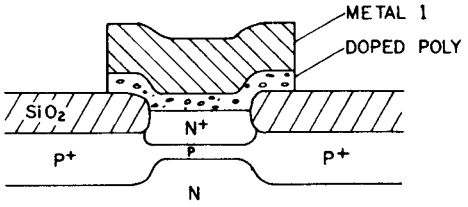

Figure 3 Polycrystalline Arsenic Emitter

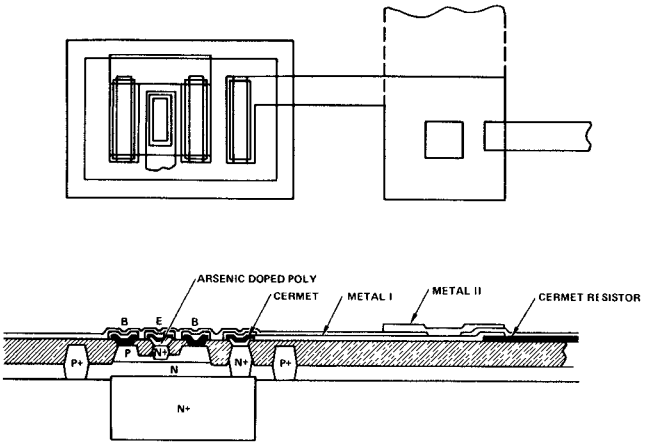

Figure 4 Complete OAT Structure

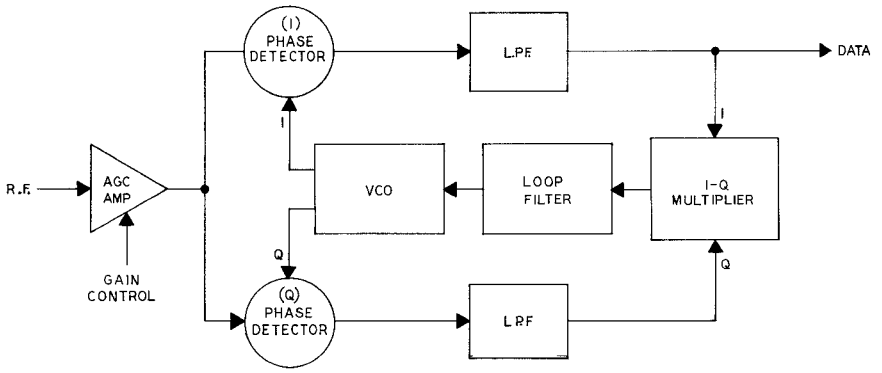

Figure 5 RF LSI Costas Demodulator

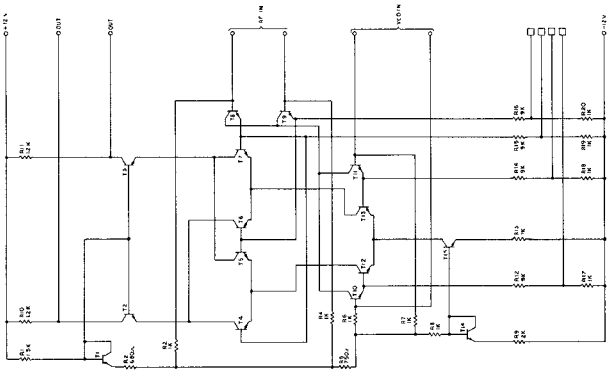

Figure 6 RF IQ Multiplier and Phase Detector